REMARKS

Summary of Office Action

Claims 1-37 are pending in the above-identified patent application.

Claims 1, 6, 8, 9, and 19 are objected to because of informalities.

Claims 1, 2, 6-10, 16-18, and 22-26 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Lee et al. U.S. Patent No. 6,266,799 (hereinafter "Lee").

Claim 11 was rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee in view of Li et al. U.S. Patent No. 6,693,985 (hereinafter "Li").

Claims 12-15 were rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee in view of Li and further in view of Wang et al. U.S. Patent No. 6,292,116 (hereinafter "Wang").

Claims 3-5, 19-21, and 27-37 were objected to as being dependent on rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of their respective base claims and any intervening claims.

Reconsideration of this application in light of the following remarks is hereby respectfully requested.

Summary of Applicants' Reply

Applicants note with appreciation the indication of allowability of claims 3-5, 19-21, and 27-37. Applicants expressly reserve the right to rewrite claims 3-5, 19-21, and 27-37 in independent form should their base claims ultimately not be allowed.

Claims 1-37 were pending in the present application. In this Reply, clarifying amendments are being

made to claims 1, 6, 8, 9, and 19. Accordingly, claims 1-37 continue to be pending in the application.

Applicants submit that claims 1-37 are allowable, as discussed below.

The §102 and §103 Rejections

Claims 1, 2, 6-10, 16-18, and 22-26 were rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Lee. Claim 11 was rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee in view of Li. Claims 12-15 were rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee in view of Li and further in view of Wang. The Examiner's rejections are respectfully traversed.

Applicants submit that the arguments presented by applicants in a Reply to Office Action mailed December 8, 2005 in this case (and submitted to the Office in response to the Examiner's Action of September 12, 2005) overcome the Examiner's pending rejections of the claims. Applicants re-submit, below, arguments substantially identical to the arguments submitted to the Office on December 8, 2005. Applicants respectfully request that the Examiner's rejections be withdrawn in view of the arguments below.

Claims 1, 2, 6-18, and 22-24

Applicants' invention, as defined by independent claims 1 and 16, is directed to circuitry and a method for extracting data from a data signal having a data rate that is twice the frequency of a reference clock signal. A first phase-shifted version of the reference clock signal is derived that is synchronized with a rising edge (i.e., a 0-to-1 level transition) of the data signal. The data signal is sampled in a predetermined phase relationship to this

first phase-shifted version to extract a first partial stream of data. A second phase-shifted version of the reference clock signal is also derived that is synchronized with a falling edge (i.e., a 1-to-0 level transition) of the data signal. The data signal is further sampled in a predetermined phase relationship to this second phase-shifted version to extract a second partial stream of data.

Contrary to the Examiner's contentions, applicants respectfully submit that Lee does not show or suggest deriving first and second versions of the reference clock signal "that are respectively synchronized with oppositely polarized transitions in level of the data signal" as recited in applicants' independent claims 1 and 16.

Lee describes "methods and apparatus for implementing data/clock recovery systems in networking circuitry" (Lee, col. 1, lines 16-20). As shown and described in connection with FIGS. 2 and 3 of Lee, a multi-phase clock generator 204 generates multiple clock phases that are sent as input to a multi-phase data/clock recover unit 110(a). Unit 110(a) selects four of the clock phases (M0, M1, M2, and M3), samples the incoming data using the selected clock phases, determines whether the clock is leading or lagging the incoming data, and accordingly adjusts the clock by selecting another set of four clock phases. The data output from unit 110(a) is based on recovered clock phases M0 and M3. (Lee, FIGS. 2 and 3; and col. 5, line 23 to col. 6, line 43).

As shown and described in connection with FIG. 5 of Lee, the clock phase M0 is mapped to the center of a first bit (data 0), the clock phase M3 is mapped to the center of a second bit (data 1), the clock phase M1 is mapped to a location just before a data transition from the first bit to

the second bit (i.e., a rising edge), and the clock phase M2 is mapped to a location just after the same data transition. All four clock phases are used to determine whether the clock phases are synchronized with the incoming data. (Lee, col. 7, lines 9-42).

In Lee, the four clock phases are respectively synchronized to the centers of each data bit, to a location just before a rising edge, and to a location just after a rising edge of the incoming data. Lee does not show or suggest one clock phase being synchronized with a rising edge and another clock phase being synchronized with a falling edge of the incoming data (i.e., "synchronized with oppositely polarized transitions in level of the data signal") as recited in applicants' independent claims 1 and 16.

For at least the foregoing reasons, applicants respectfully submit that independent claims 1 and 16 are allowable. Claims 2, 6-15, 17, 18, and 22-24, which each depend from one of independent claims 1 and 16, are therefore also allowable.

Claims 25 and 26

Applicants' invention, as defined by independent claim 25, is directed to an apparatus for receiving an information signal that includes data information and clock information for the data information embedded in the information signal. The apparatus includes first input circuitry to receive the information signal and second input circuitry to receive a reference clock signal. Reference clock signal processing circuitry produces two recovered clock signals based on the information signal and the reference clock signal, the two recovered clock signals being respectively synchronized with oppositely polarized

transitions in level of the information signal. Data recovery circuitry produces two retimed data output signals indicative of the data information in the information signal based on the information signal and the two recovered clock signals.

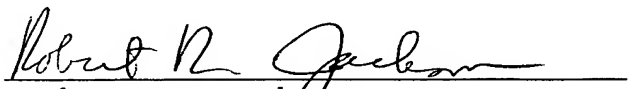
For at least the reasons given above with respect to independent claims 1 and 16, applicants respectfully submit that independent claim 25 is also allowable. Claim 26, which depends from independent claim 25, is therefore also allowable.

Conclusion

In view of the foregoing, applicants respectfully submit that this application, including claims 1-37, is in condition for allowance. Reconsideration and allowance of this application are respectfully requested.

An early and favorable action is respectfully requested.

Respectfully submitted,



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